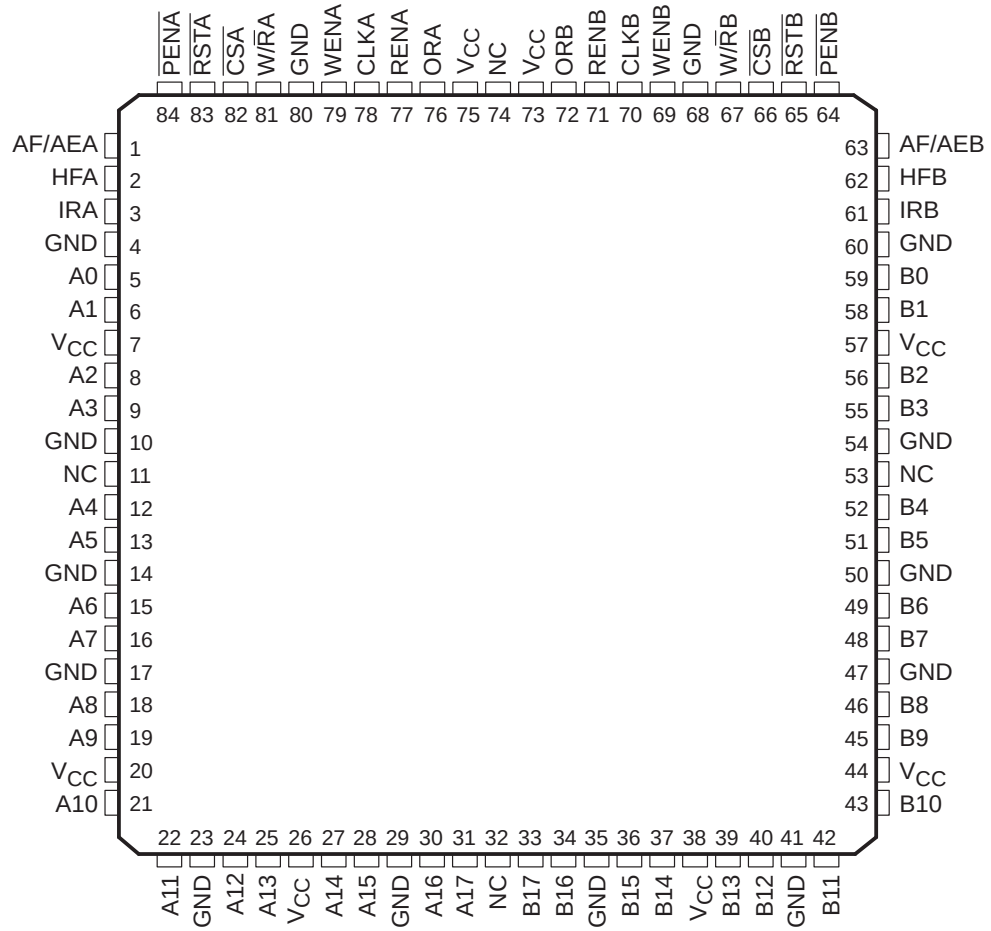
- Member of the Texas Instruments Widebus™ Family
- Advanced BiCMOS Technology
- Free-Running CLKA and CLKB Can Be Asynchronous or Coincident
- Read and Write Operations Synchronized to Independent System Clocks
- Two Separate 512 × 18 Clocked FIFOs Buffering Data in Opposite Directions
- IRA and ORA Synchronized to CLKA
- IRB and ORB Synchronized to CLKB
- Microprocessor Interface Control Logic
- Programmable Almost-Full/Almost-Empty Flag
- Fast Access Times of 9 ns With a 50-pF Load and Simultaneous-Switching Data Outputs
- Released as DSCC SMD (Standard Microcircuit Drawing) 5962-9470401QXA and 5962-9470401QYA
- Package Options Include 84-Pin Ceramic Pin Grid Array (GB) and 84-Pin Ceramic Quad Flat (HT) Package

HT PACKAGE
(TOP VIEW)



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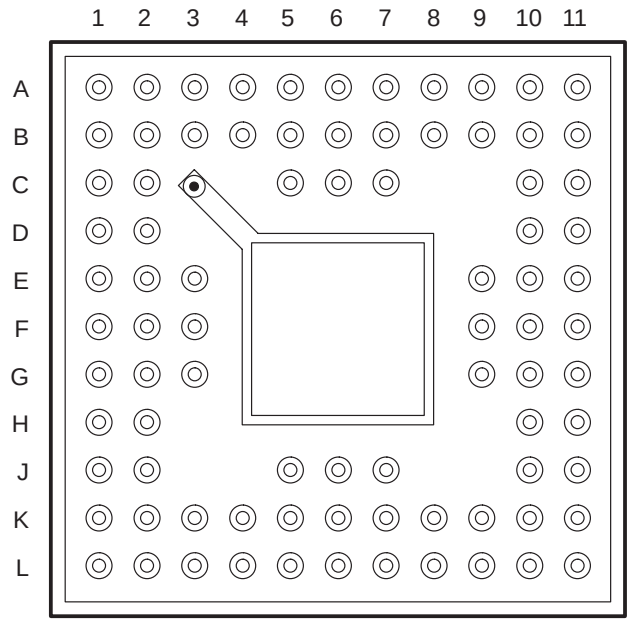
Widebus is a trademark of Texas Instruments Incorporated.

GB PACKAGE
(TOP VIEW)



Terminal Assignments

TERMINAL	NAME	TERMINAL	NAME	TERMINAL	NAME	TERMINAL	NAME
A1	$\overline{\text{PENA}}$	B11	IRB	F9	NC	K2	A11
A2	$\overline{\text{CSA}}$	C1	GND	F10	B6	K3	GND
A3	W/$\overline{\text{R}}$A	C2	HFA	F11	GND	K4	V_{CC}
A4	WENA	C5	CLKA	G1	A5	K5	GND
A5	ORA	C6	NC	G2	GND	K6	A17
A6	V_{CC}	C7	V_{CC}	G3	A4	K7	GND
A7	ORB	C10	HFB	G9	B4	K8	V_{CC}
A8	WENB	C11	GND	G10	GND	K9	GND
A9	W/$\overline{\text{R}}$B	D1	A1	G11	B5	K10	B10
A10	$\overline{\text{CSB}}$	D2	A0	H1	A7	K11	B9
A11	AF/AEB	D10	B0	H2	GND	L1	A10
B1	IRA	D11	B1	H10	GND	L2	A12
B2	AF/AEA	E1	A3	H11	B7	L3	A13
B3	$\overline{\text{RSTA}}$	E2	A2	J1	A8	L4	A14
B4	GND	E3	V_{CC}	J2	V_{CC}	L5	A16
B5	RENA	E9	V_{CC}	J5	A15	L6	B15
B6	CLKB	E10	B2	J6	NC	L7	B16
B7	RENB	E11	B3	J7	B17	L8	B14
B8	GND	F1	A6	J10	V_{CC}	L9	B13
B9	$\overline{\text{RSTB}}$	F2	GND	J11	B8	L10	B12
B10	$\overline{\text{PENB}}$	F3	NC	K1	A9	L11	B11

description

A FIFO memory is a storage device that allows data to be read from its array in the same order it is written. The SN54ABT7819 is a high-speed, low-power BiCMOS bidirectional clocked FIFO memory. Two independent 512 × 18 dual-port SRAM FIFOs on the chip buffer data in opposite directions. Each FIFO has flags to indicate empty and full conditions, a half-full flag, and a programmable almost-full/almost-empty flag.

The SN54ABT7819 is a clocked FIFO, which means each port employs a synchronous interface. All data transfers through a port are gated to the low-to-high transition of a continuous (free-running) port clock by enable signals. The continuous clocks for each port are independent of one another and can be asynchronous or coincident. The enables for each port are arranged to provide a simple bidirectional interface between microprocessors and/or buses with synchronous control.

The state of the A0–A17 outputs is controlled by $\overline{CSA}$ and W/$\overline{R}$A. When both $\overline{CSA}$ and W/$\overline{R}$A are low, the outputs are active. The A0–A17 outputs are in the high-impedance state when either $\overline{CSA}$ or W/$\overline{R}$A is high. Data is written to FIFOA–B from port A on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is high, WENA is high, and the IRA flag is high. Data is read from FIFOB–A to the A0–A17 outputs on the low-to-high transition of CLKA when $\overline{CSA}$ is low, W/$\overline{R}$A is low, RENA is high, and the ORA flag is high.

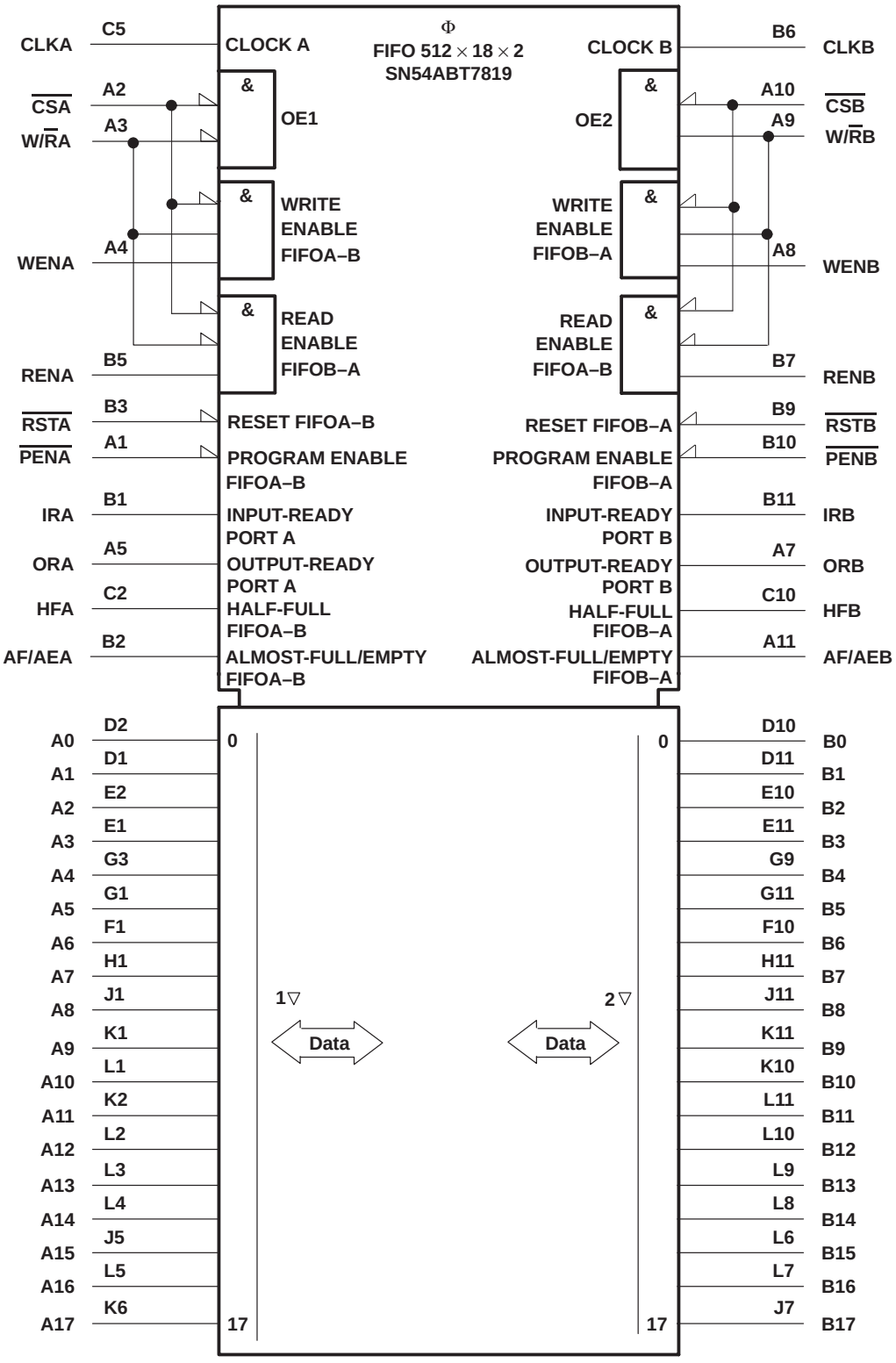
The state of the B0–B17 outputs is controlled by $\overline{CSB}$ and W/$\overline{R}$B. When both $\overline{CSB}$ and W/$\overline{R}$B are low, the outputs are active. The B0–B17 outputs are in the high-impedance state when either $\overline{CSB}$ or W/$\overline{R}$B is high. Data is written to FIFOB–A from port B on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is high, WENB is high, and the IRB flag is high. Data is read from FIFOA–B to the B0–B17 outputs on the low-to-high transition of CLKB when $\overline{CSB}$ is low, W/$\overline{R}$B is low, RENB is high, and the ORB flag is high.

The setup- and hold-time constraints for the chip selects ($\overline{CSA}$, $\overline{CSB}$) and write/read selects (W/$\overline{R}$A, W/$\overline{R}$B) enable and read operations on memory and are not related to the high-impedance control of the data outputs. If a port read enable (RENA or RENB) and write enable (WENA or WENB) are set low during a clock cycle, the chip select and write/read select can switch at any time during the cycle to change the state of the data outputs.

The input-ready and output-ready flags of a FIFO are two-stage synchronized to the port clocks for use as reliable control signals. CLKA synchronizes the status of the input-ready flag of FIFOA–B (IRA) and the output-ready flag of FIFOB–A (ORA). CLKB synchronizes the status of the input-ready flag of FIFOB–A (IRB) and the output-ready flag of FIFOA–B (ORB). When the input-ready flag of a port is low, the FIFO receiving input from the port is full and writes are disabled to its array. When the output-ready flag of a port is low, the FIFO that outputs data to the port is empty and reads from its memory are disabled. The first word loaded to an empty memory is sent to the FIFO output register at the same time its output-ready flag is asserted (high). When the memory is read empty and the output-ready flag is forced low, the last valid data remains on the FIFO outputs until the output-ready flag is asserted (high) again. In this way, a high on the output-ready flag indicates new data is present on the FIFO outputs.

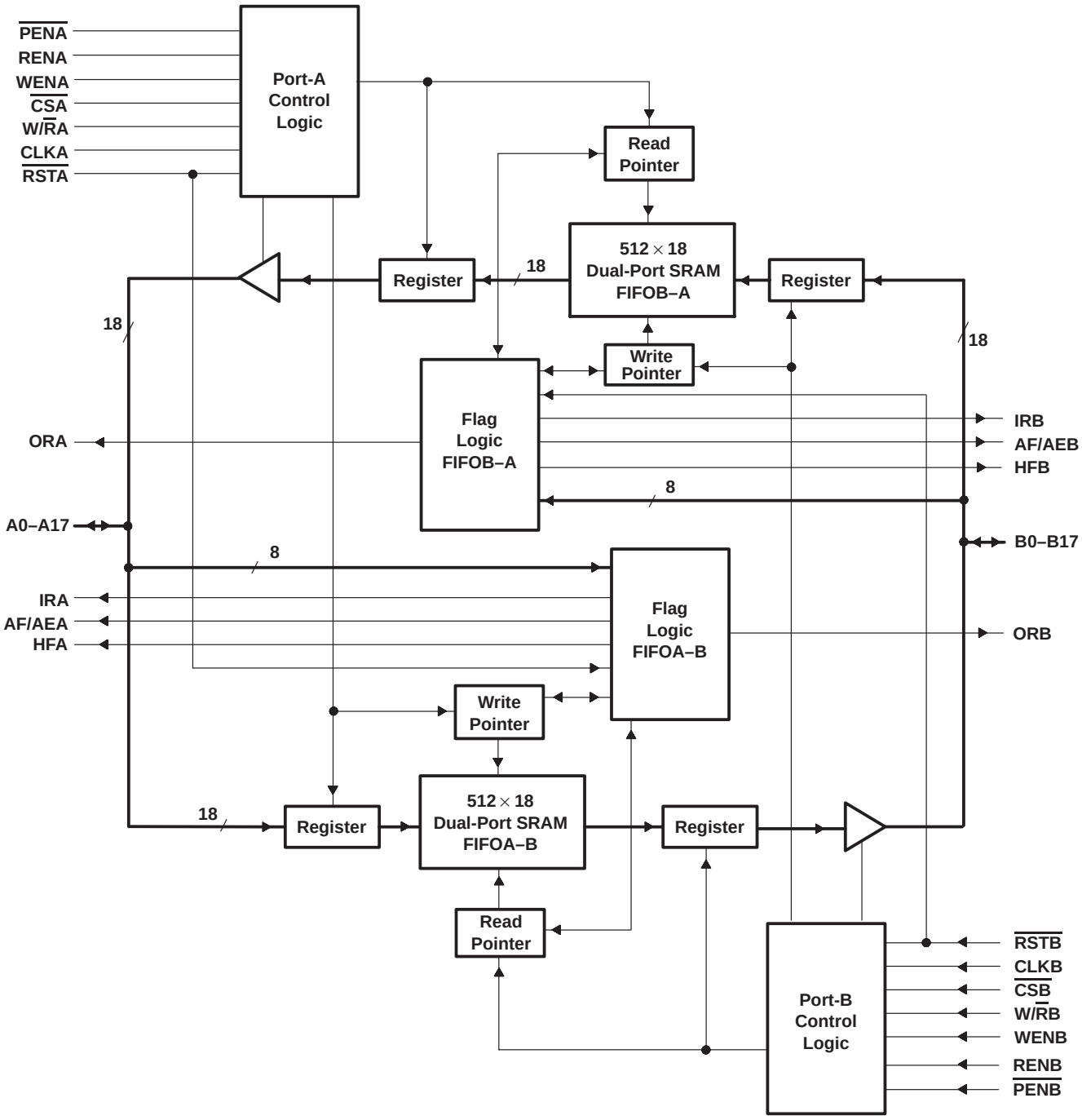
The SN54ABT7819 is characterized for operation over the full military temperature range of –55°C to 125°C.

logic symbol†

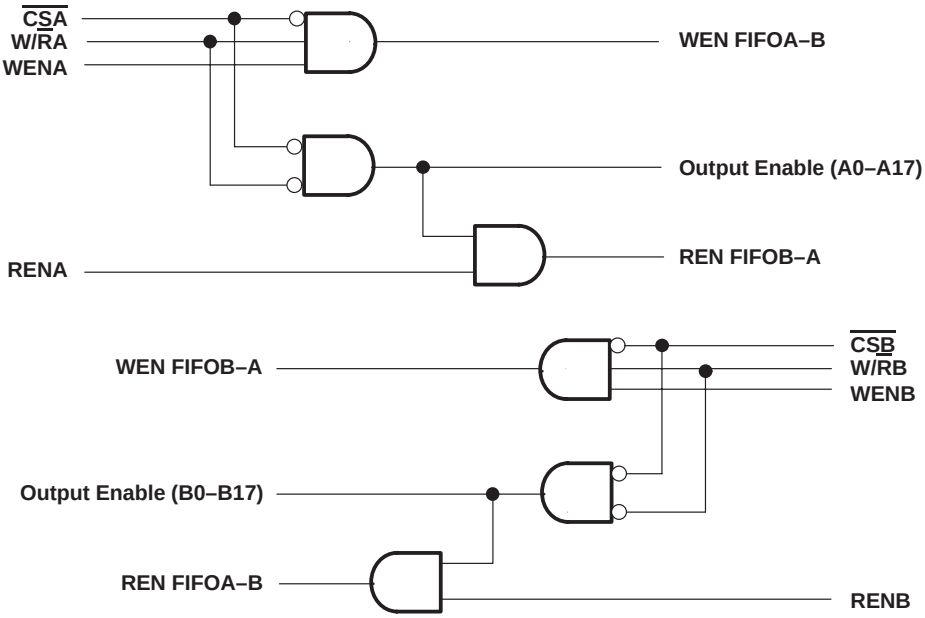


† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.
Pin numbers shown are for the GB package.

functional block diagram



enable logic diagram (positive logic)



Function Tables

A PORT

SELECT INPUTS					A0–A17	OPERATION
CLKA	$\overline{CSA}$	W/$\overline{RA}$	WENA	RENA		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write A0–A17 to FIFOA–B
↑	L	L	X	H	Active	Read FIFOB–A to A0–A17

B PORT

SELECT INPUTS					B0–B17	OPERATION
CLKB	$\overline{CSB}$	W/$\overline{RB}$	WENB	RENB		
X	H	X	X	X	High Z	None
↑	L	H	H	X	High Z	Write B0–B17 to FIFOB–A
↑	L	L	X	H	Active	Read FIFOA–B to B0–B17

Terminal Functions

TERMINAL NAME	I/O	DESCRIPTION
A0–A17	I/O	Port-A data. The 18-bit bidirectional data port for side A.
AF/AEA	O	FIFOA–B almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEA, or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEA is high when X or fewer words or (512 – Y) or more words are stored in FIFOA–B. AF/AEA is forced high when FIFOA–B is reset.
AF/AEB	O	FIFOB–A almost-full/almost-empty flag. Depth offsets can be programmed for AF/AEB, or the default value of 128 can be used for both the almost-empty offset (X) and the almost-full offset (Y). AF/AEB is high when X or fewer words or (512 – Y) or more words are stored in FIFOB–A. AF/AEB is forced high when FIFOB–A is reset.
B0–B17	I/O	Port-B data. The 18-bit bidirectional data port for side B.
CLKA	I	Port-A clock. CLKA is a continuous clock that synchronizes all data transfers through port A to its low-to-high transition and can be asynchronous or coincident to CLKB.
CLKB	I	Port-B clock. CLKB is a continuous clock that synchronizes all data transfers through port B to its low-to-high transition and can be asynchronous or coincident to CLKA.
$\overline{\text{CSA}}$	I	Port-A chip select. $\overline{\text{CSA}}$ must be low to enable a low-to-high transition of CLKA to either write data from A0–A17 to FIFOA–B or read data from FIFOB–A to A0–A17. The A0–A17 outputs are in the high-impedance state when $\overline{\text{CSA}}$ is high.
$\overline{\text{CSB}}$	I	Port-B chip select. $\overline{\text{CSB}}$ must be low to enable a low-to-high transition of CLKB to either write data from B0–B17 to FIFOB–A or read data from FIFOA–B to B0–B17. The B0–B17 outputs are in the high-impedance state when $\overline{\text{CSB}}$ is high.
HFA	O	FIFOA–B half-full flag. HFA is high when FIFOA–B contains 256 or more words and is low when FIFOA–B contains 255 or fewer words. HFA is set low after FIFOA–B is reset.
HFB	O	FIFOB–A half-full flag. HFB is high when FIFOB–A contains 256 or more words and is low when FIFOB–A contains 255 or fewer words. HFB is set low after FIFOB–A is reset.
IRA	O	Port-A input-ready flag. IRA is synchronized to the low-to-high transition of CLKA. When IRA is low, FIFOA–B is full and writes to its array are disabled. IRA is set low during a FIFOA–B reset and is set high on the second low-to-high transition of CLKA after reset.
IRB	O	Port-B input-ready flag. IRB is synchronized to the low-to-high transition of CLKB. When IRB is low, FIFOB–A is full and writes to its array are disabled. IRB is set low during a FIFOB–A reset and is set high on the second low-to-high transition of CLKB after reset.
ORA	O	Port-A output-ready flag. ORA is synchronized to the low-to-high transition of CLKA. When ORA is low, FIFOB–A is empty and reads from its array are disabled. The last valid word remains on the FIFOB–A outputs when ORA is low. Ready data is present for the A0–A17 outputs when ORA is high. ORA is set low during a FIFOB–A reset and goes high on the third low-to-high transition of CLKA after the first word is loaded to an empty FIFOB–A.
ORB	O	Port-B output-ready flag. ORB is synchronized to the low-to-high transition of CLKB. When ORB is low, FIFOA–B is empty and reads from its array are disabled. The last valid word remains on the FIFOA–B outputs when ORB is low. Ready data is present for the B0–B17 outputs when ORB is high. ORB is set low during a FIFOA–B reset and goes high on the third low-to-high transition of CLKB after the first word is loaded to an empty FIFOA–B.
$\overline{\text{PENA}}$	I	AF/AEA program enable. After FIFOA–B is reset and before a word is written to its array, the binary value on A0–A7 is latched as an AF/AEA offset when $\overline{\text{PENA}}$ is low and CLKA is high.
$\overline{\text{PENB}}$	I	AF/AEB program enable. After FIFOB–A is reset and before a word is written to its array, the binary value on B0–B7 is latched as an AF/AEB offset when $\overline{\text{PENB}}$ is low and CLKB is high.
RENA	I	Port-A read enable. A high level on RENA enables data to be read from FIFOB–A on the low-to-high transition of CLKA when $\overline{\text{CSA}}$ is low, W/$\overline{\text{R}}$A is low, and ORA is high.
RENB	I	Port-B read enable. A high level on RENB enables data to be read from FIFOA–B on the low-to-high transition of CLKB when $\overline{\text{CSB}}$ is low, W/$\overline{\text{R}}$B is low, and ORB is high.
$\overline{\text{RSTA}}$	I	FIFOA–B reset. To reset FIFOA–B, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RSTA}}$ is low. This sets HFA low, IRA low, ORB low, and AF/AEA high.
$\overline{\text{RSTB}}$	I	FIFOB–A reset. To reset FIFOB–A, four low-to-high transitions of CLKA and four low-to-high transitions of CLKB must occur while $\overline{\text{RSTB}}$ is low. This sets HFB low, IRB low, ORA low, and AF/AEB high.

Terminal Functions (Continued)

TERMINAL NAME	I/O	DESCRIPTION
WENA	I	Port-A write enable. A high level on WENA enables data on A0–A17 to be written into FIFOA–B on the low-to-high transition of CLKA when W/$\overline{R}$A is high, $\overline{CSA}$ is low, and IRA is high.
WENB	I	Port-B write enable. A high level on WENB enables data on B0–B17 to be written into FIFOB–A on the low-to-high transition of CLKB when W/$\overline{R}$B is high, $\overline{CSB}$ is low, and IRB is high.
W/$\overline{R}$A	I	Port-A write/read select. A high on W/$\overline{R}$A enables A0–A17 data to be written to FIFOA–B on a low-to-high transition of CLKA when WENA is high, $\overline{CSA}$ is low, and IRA is high. A low on W/$\overline{R}$A enables data to be read from FIFOB–A on a low-to-high transition of CLKA when RENA is high, $\overline{CSA}$ is low, and ORA is high. The A0–A17 outputs are in the high-impedance state when W/$\overline{R}$A is high.
W/$\overline{R}$B	I	Port-B write/read select. A high on W/$\overline{R}$B enables B0–B17 data to be written to FIFOB–A on a low-to-high transition of CLKB when WENB is high, $\overline{CSB}$ is low, and IRB is high. A low on W/$\overline{R}$B enables data to be read from FIFOA–B on a low-to-high transition of CLKB when RENB is high, $\overline{CSB}$ is low, and ORB is high. The B0–B17 outputs are in the high-impedance state when W/$\overline{R}$B is high.

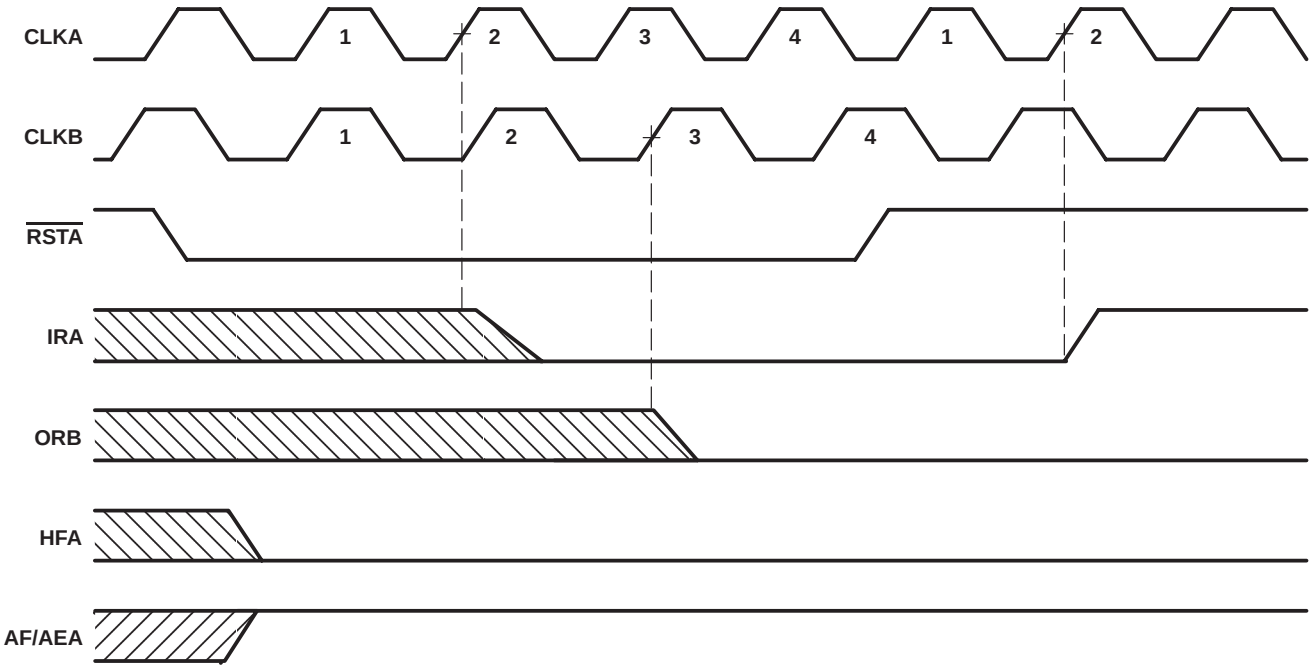
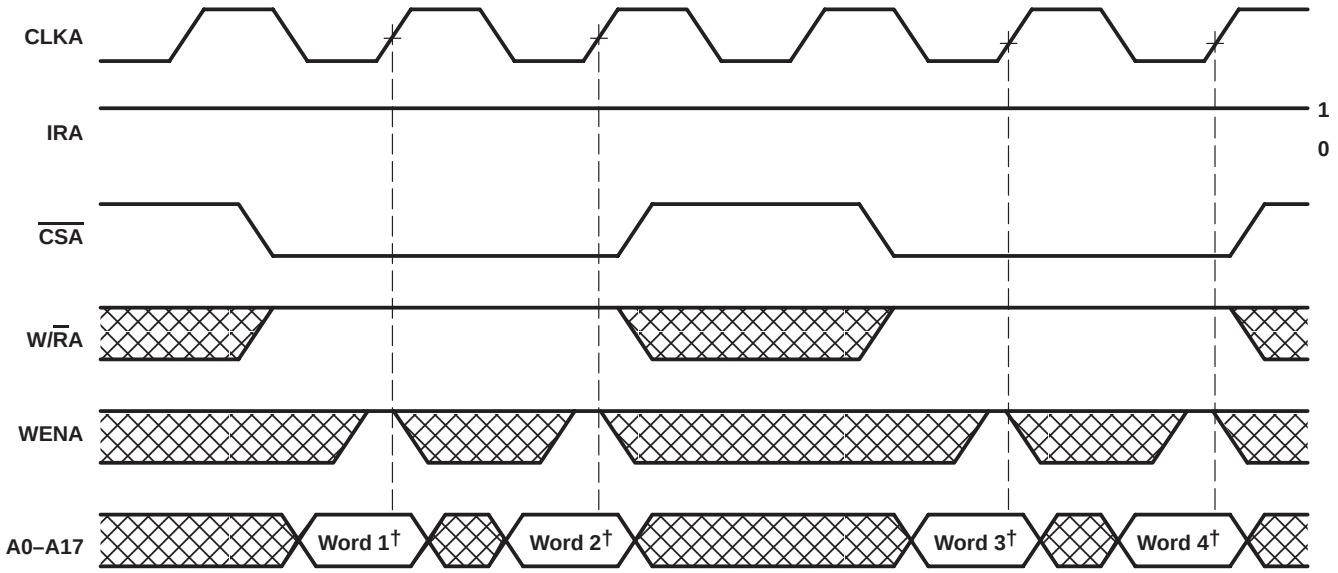


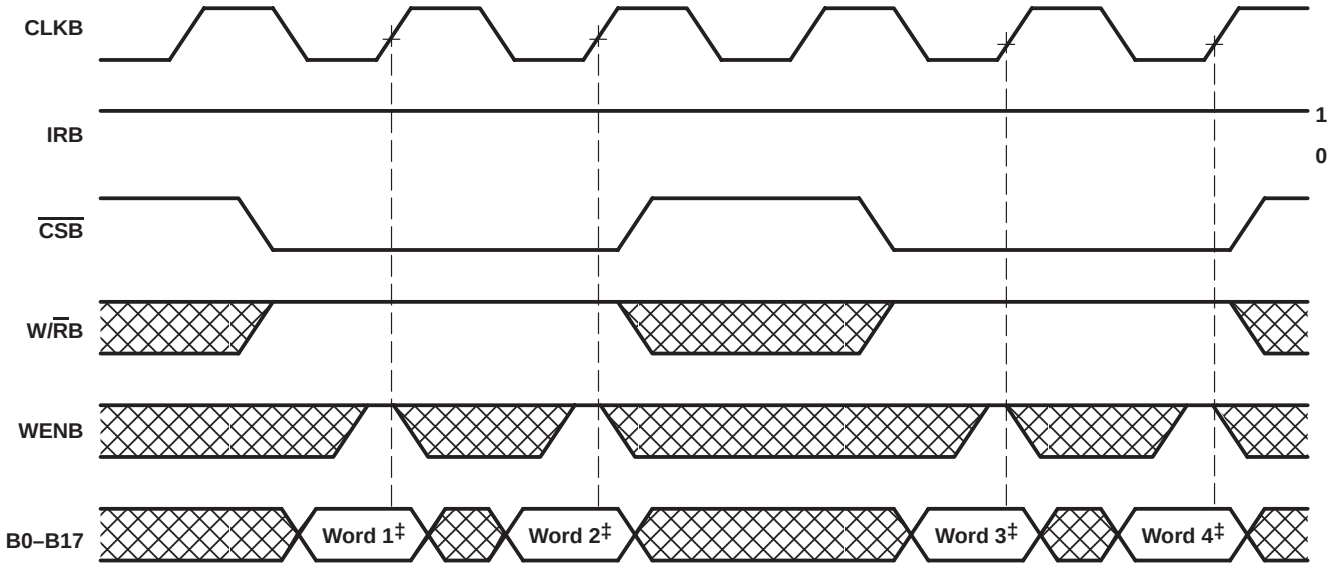
Figure 1. Reset Cycle for FIFOA–B†

† FIFOB–A is reset in the same manner.



† Written to FIFOA–B

Figure 2. Write Timing – Port A



‡ Written to FIFOB–A

Figure 3. Write Timing – Port B

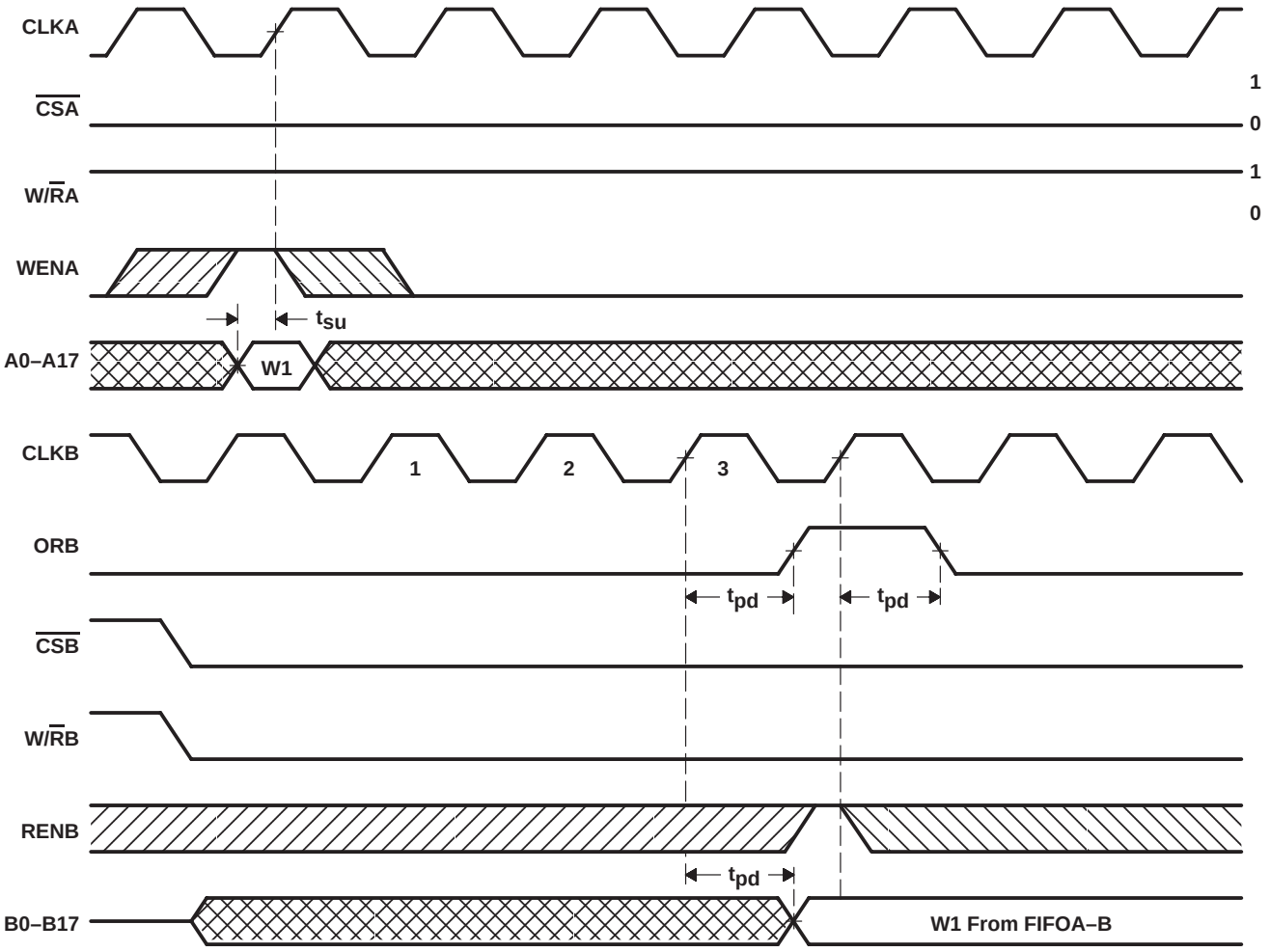


Figure 4. ORB-Flag Timing and First Data-Word Fall-Through When FIFOA–B Is Empty†

† Operation of FIFOB–A is identical to that of FIFOA–B.

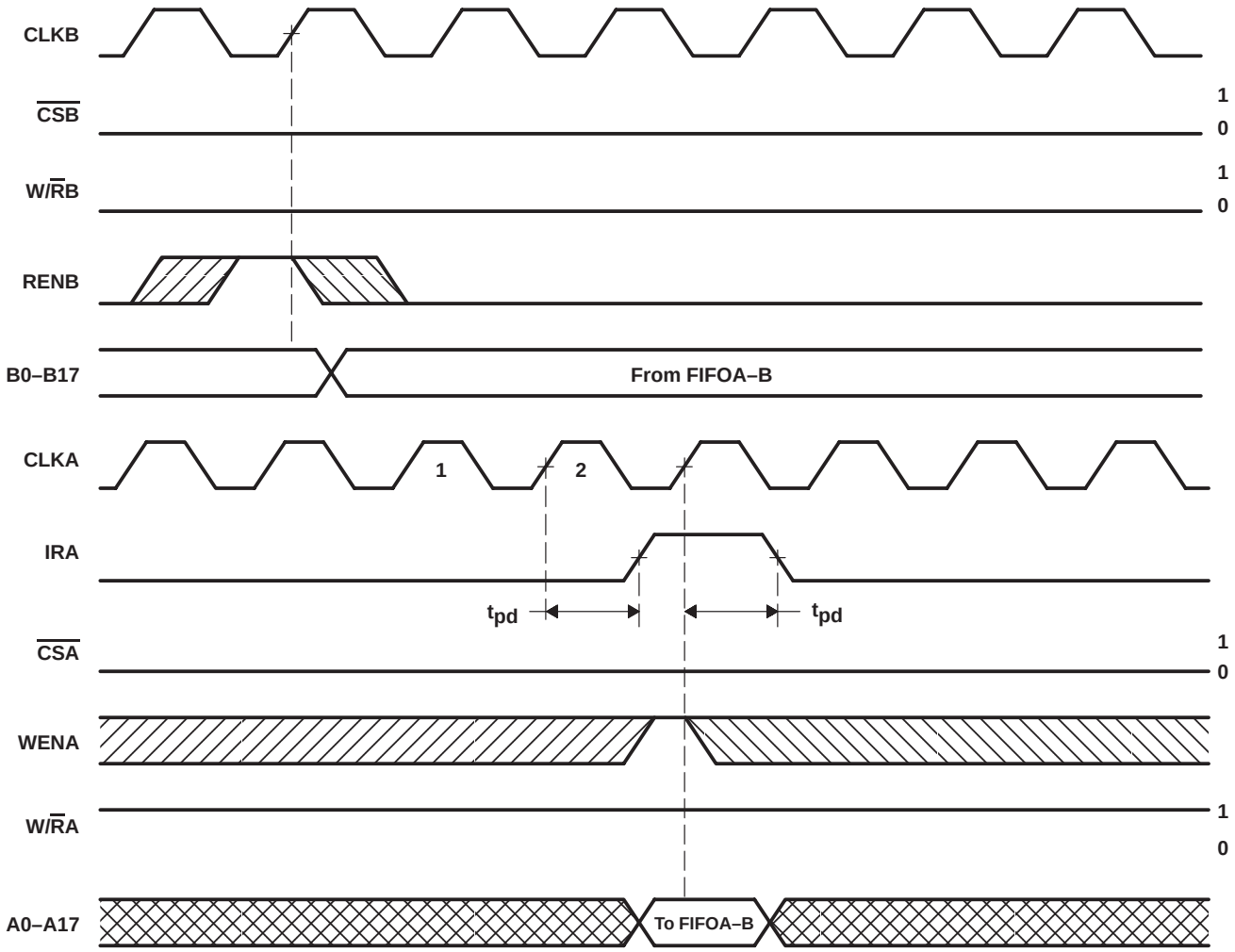
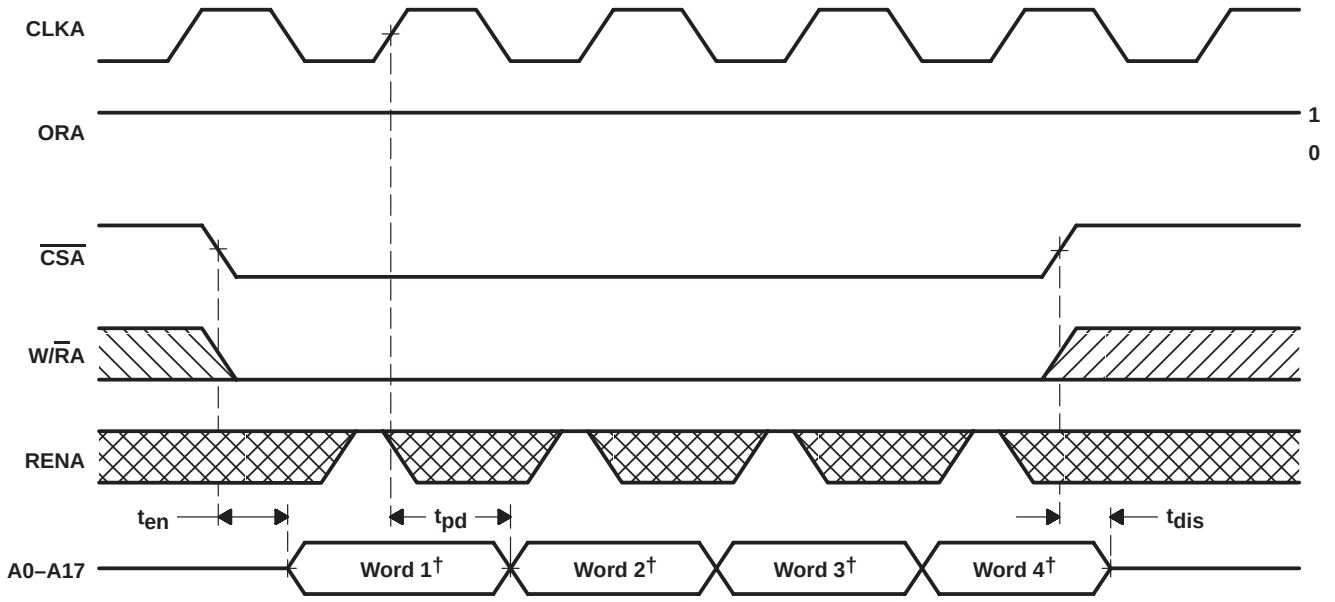


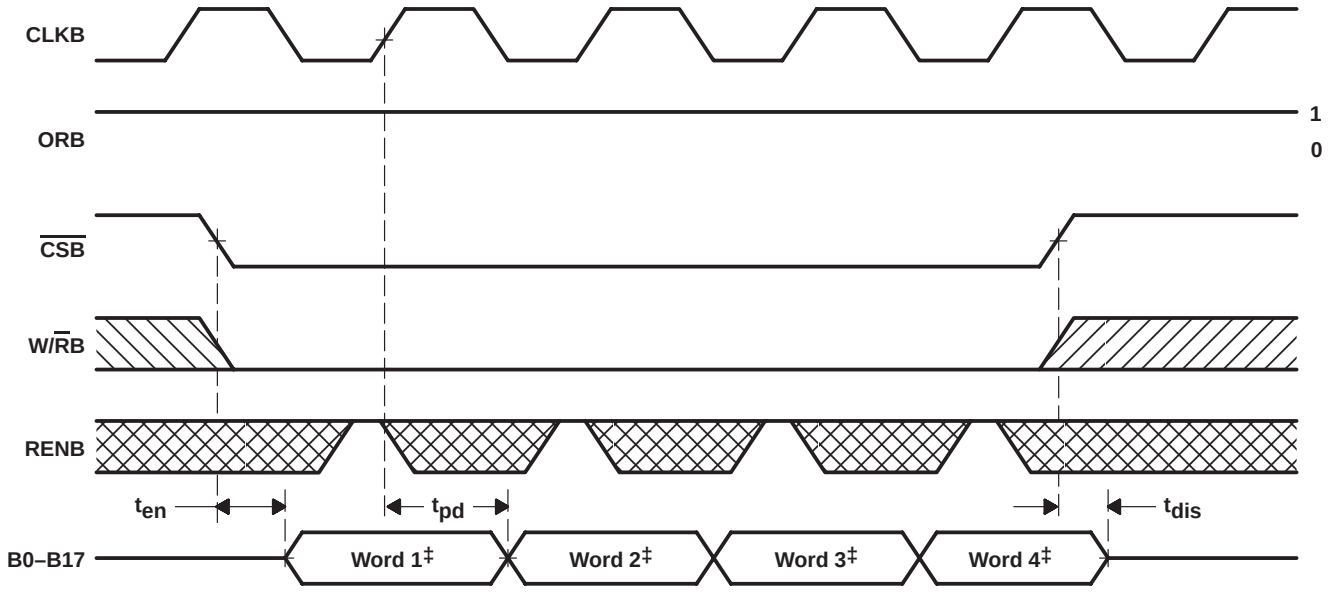
Figure 5. Write-Cycle and IRA-Flag Timing When FIFOA–B Is Full†

† Operation of FIFOB–A is identical to that of FIFOA–B.



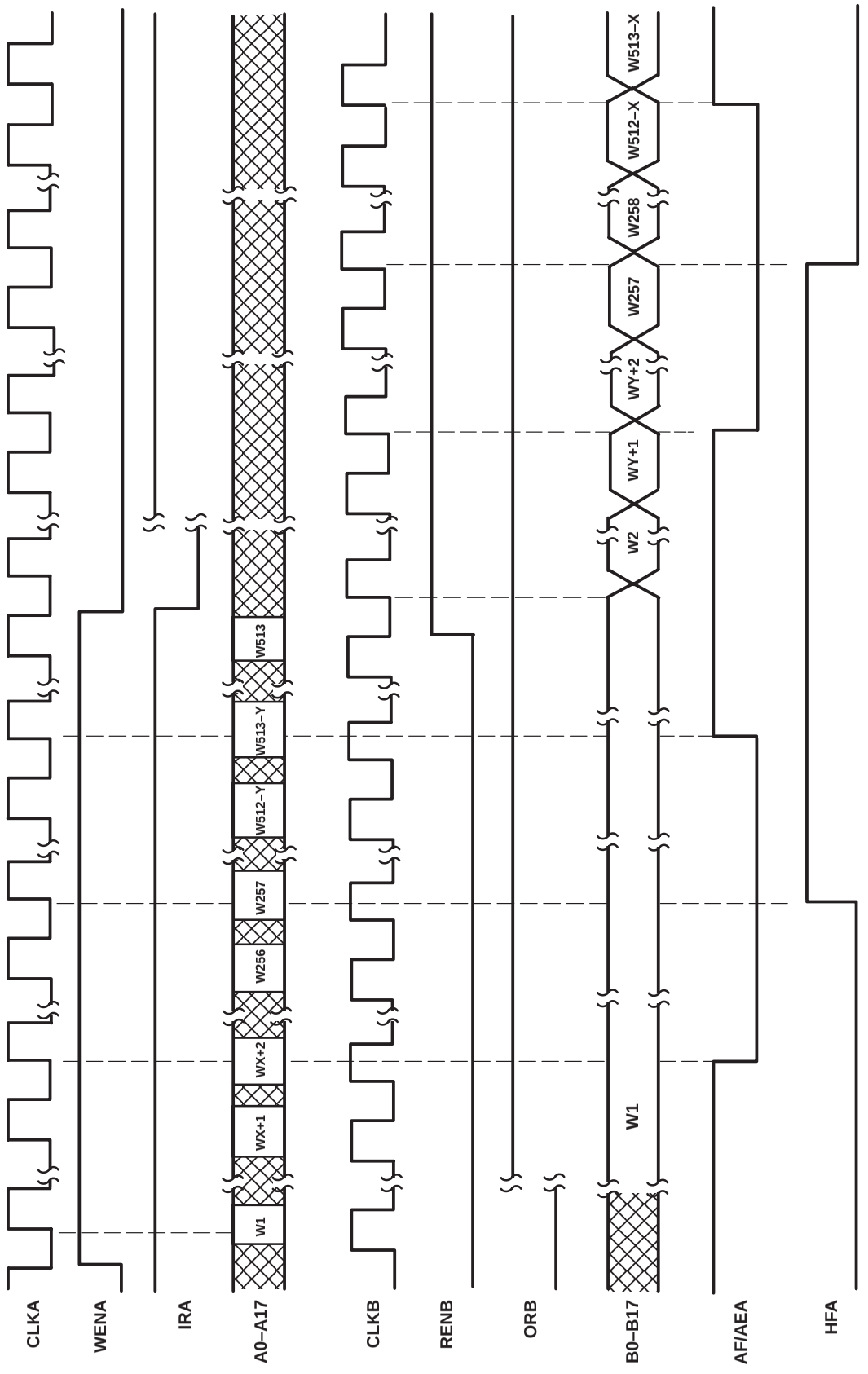
† Read from FIFOB–A

Figure 6. Read Timing – Port A



‡ Read from FIFOA–B

Figure 7. Read Timing – Port B



NOTES: A. $\overline{CSA}$, $\overline{CSB}$ = 0, W/$\overline{RA}$ = 1, W/$\overline{RB}$ = 0
B. X is the almost-empty offset and Y is the almost-full offset for AF/AEA.
C. HFB and AF/AEB function in the same manner for FIFO B – A.

Figure 8. FIFOA – B (HFA, AF/AEA) Asynchronous Flag Timing

offset values for AF/AE

The AF/AE flag of each FIFO has two programmable limits: the almost-empty offset value (X) and the almost-full offset value (Y). They can be programmed from the input of the FIFO after it is reset and before a word is written to its memory. An AF/AE flag is high when its FIFO contains X or fewer words or (512 – Y) or more words.

To program the offset values for AF/AEA, $\overline{\text{PENA}}$ can be brought low after FIFOA–B is reset and only when CLKA is low. On the following low-to-high transition of CLKA, the binary value on A0–A7 is stored as the almost-empty offset value (X) and the almost-full offset value (Y). Holding $\overline{\text{PENA}}$ low for another low-to-high transition of CLKA reprograms Y to the binary value on A0–A7 at the time of the second CLKA low-to-high transition.

During the first two CLKA cycles used for offset programming, $\overline{\text{PENA}}$ can be brought high only when CLKA is low. $\overline{\text{PENA}}$ can be brought high at any time after the second CLKA pulse used for offset programming returns low. A maximum value of 255 can be programmed for either X or Y (see Figure 9). To use the default values of X = Y = 128, $\overline{\text{PENA}}$ must be tied high. No data is stored in FIFOA–B while the AF/AEA offsets are programmed. The AF/AEB flag is programmed in the same manner, with $\overline{\text{PENB}}$ enabling CLKB to program the offset values taken from B0–B7.

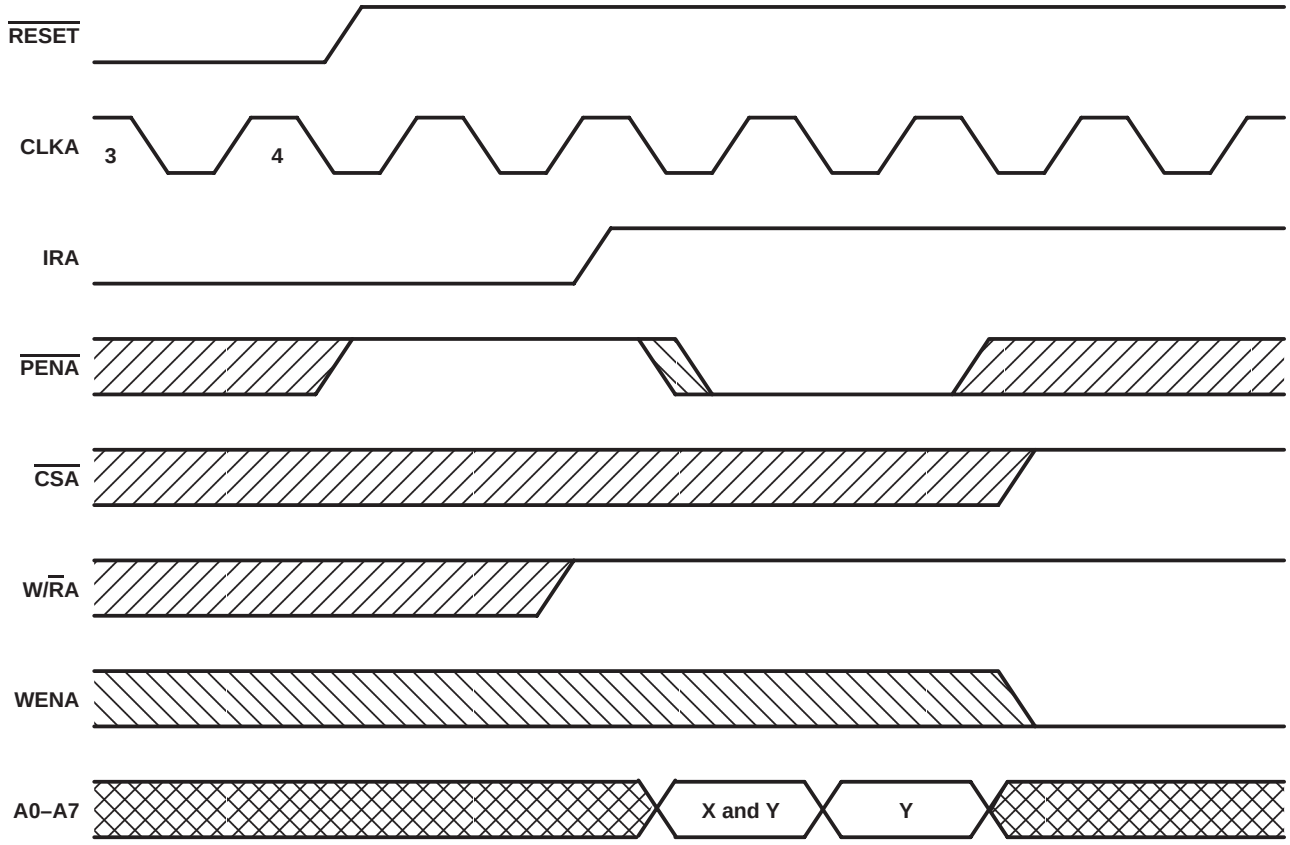


Figure 9. Programming X and Y Separately for AF/AEA

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . –0.5 V to 7 V
Input voltage range, V_I (see Note 1) . . . . . –0.5 V to V_{CC} + 0.5 V
Voltage range applied to any output in the high state or power-off state, V_O . . . . . –0.5 V to 5.5 V
Current into any output in the low state, I_O . . . . . 48 mA
Input clamp current, I_{IK} (V_I < 0) . . . . . –18 mA
Output clamp current, I_{OK} (V_O < 0) . . . . . –50 mA
Storage temperature range, T_{stg} . . . . . –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2			V
V_{IL}	Low-level input voltage			0.8	V
V_I	Input voltage	0		V_{CC}	V
I_{OH}	High-level output current			–12	mA
I_{OL}	Low-level output current			24	mA
$\Delta t/\Delta v$	Input transition rise or fall rate			5	ns/V
T_A	Operating free-air temperature	–55		125	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP‡	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –3 mA		2.5			V
		V_{CC} = 5 V,	I_{OH} = –3 mA		3			
		V_{CC} = 4.5 V,	I_{OH} = –12 mA		2			
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.5	0.55	V
I_I		V_{CC} = 5.5 V,	V_I = V_{CC} or GND				±1	µA
I_{OZH}§		V_{CC} = 5.5 V,	V_O = 2.7 V				50	µA
I_{OZL}§		V_{CC} = 5.5 V,	V_O = 0.5 V				– 50	µA
I_O¶		V_{CC} = 5.5 V,	V_O = 2.5 V		–40	–100	–180	mA
I_{CC}		V_{CC} = 5.5 V,	I_O = 0, V_I = V_{CC} or GND	Outputs high			15	mA
				Outputs low			95	
				Outputs disabled			15	
C_i	Control inputs	V_I = 2.5 V or 0.5 V				6		pF
C_o	Flags	V_O = 2.5 V or 0.5 V				4		pF
C_{io}	A or B ports	V_O = 2.5 V or 0.5 V				8		pF

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ The parameters I_{OZH} and I_{OZL} include the input leakage current.
¶ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 through 10)

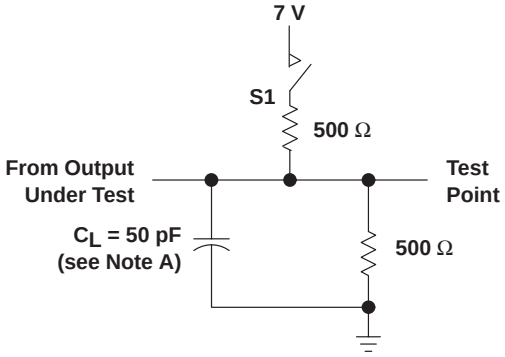
			MIN	MAX	UNIT
f_{clock}	Clock frequency			50	MHz
t_w	Pulse duration	CLKA, CLKB high or low	8		ns
t_{su}	Setup time	A0–A17 before CLKA↑ and B0–B17 before CLKB↑	5		ns
		$\overline{CSA}$ before CLKA↑ and $\overline{CSB}$ before CLKB↑	7.5		
		W/$\overline{R}$A before CLKA↑ and W/$\overline{R}$B before CLKB↑	7.5		
		WENA before CLKA↑ and WENB before CLKB↑	5		
		RENA before CLKA↑ and RENB before CLKB↑	5		
		$\overline{PENA}$ before CLKA↑ and $\overline{PENB}$ before CLKB↑	5		
		$\overline{RSTA}$ or $\overline{RSTB}$ low before first CLKA↑ and CLKB↑†	5		
t_h	Hold time	A0–A17 after CLKA↑ and B0–B17 after CLKB↑	0		ns
		$\overline{CSA}$ after CLKA↑ and $\overline{CSB}$ after CLKB↑	0		
		W/$\overline{R}$A after CLKA↑ and W/$\overline{R}$B after CLKB↑	0		
		WENA after CLKA↑ and WENB after CLKB↑	0		
		RENA after CLKA↑ and RENB after CLKB↑	0		
		$\overline{PENA}$ after CLKA low and $\overline{PENB}$ after CLKB low	3		
		$\overline{RSTA}$ or $\overline{RSTB}$ low after fourth CLKA↑ and CLKB↑†	4		

† To permit the clock pulse to be utilized for reset purposes

switching characteristics over recommended ranges of supply voltage and operating free-air temperature, C_L = 50 pF (unless otherwise noted) (see Figure 10)

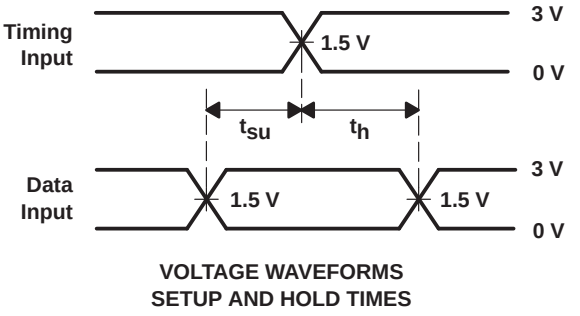
PARAMETER	FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{max}	CLKA or CLKB		50		MHz
t_{pd}	CLKA↑	A0–A17	3	12	ns
	CLKB↑	B0–B17	3	12	
	CLKA↑	IRA	3	12	
	CLKB↑	IRB	3	12	
	CLKA↑	ORA	2.5	12	
	CLKB↑	ORB	2.5	12	
	CLKA↑	AF/AEA	7	18	
	CLKB↑		7	18	
t_{PLH}	$\overline{RSTA}$	AF/AEA	3	15	ns
t_{pd}	CLKA↑	AF/AEB	7	18	ns
	CLKB↑		7	18	
t_{PLH}	$\overline{RSTB}$	AF/AEB	3	15	ns
	CLKA↑	HFA	7	18	
t_{PHL}	CLKB↑	HFA	7	18	ns
	$\overline{RSTA}$		3	15	
	CLKA↑	HFB	7	18	
t_{PLH}	CLKB↑	HFB	7	18	ns
t_{PHL}	$\overline{RSTB}$	HFB	3	15	ns
t_{en}	$\overline{CSA}$	A0–A17	1.5	10	ns
	W/$\overline{R}$A		1.5	10	
	$\overline{CSB}$	B0–B17	1.5	10	
	W/$\overline{R}$B		1.5	10	
t_{dis}	$\overline{CSA}$	A0–A17	1.5	10	ns
	W/$\overline{R}$A		1.5	10	
	$\overline{CSB}$	B0–B17	1.5	10	
	W/$\overline{R}$B		1.5	10	

PARAMETER MEASUREMENT INFORMATION

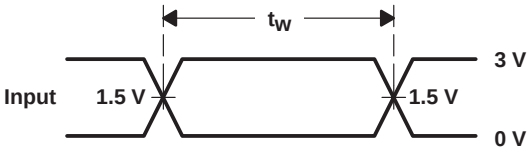


LOAD CIRCUIT

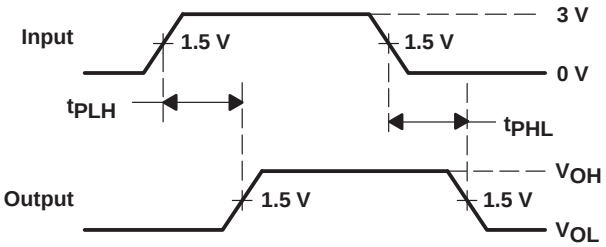
PARAMETER		S1
t_{en}	t_{PZH}	Open
	t_{PZL}	Closed
t_{dis}	t_{PHZ}	Open
	t_{PLZ}	Closed
t_{pd}	t_{PLH}	Open
	t_{PHL}	Open



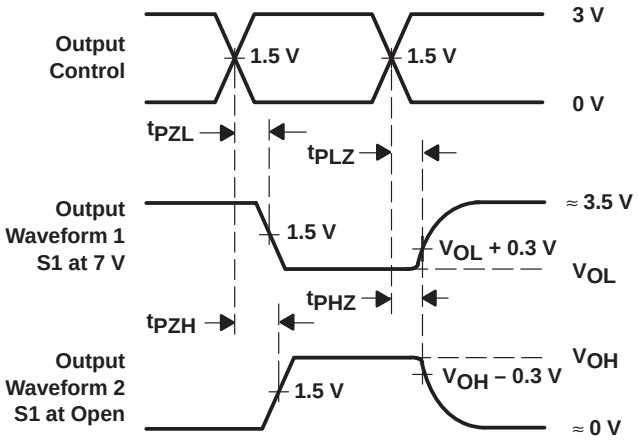
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTE A: C_L includes probe and jig capacitance.

Figure 10. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

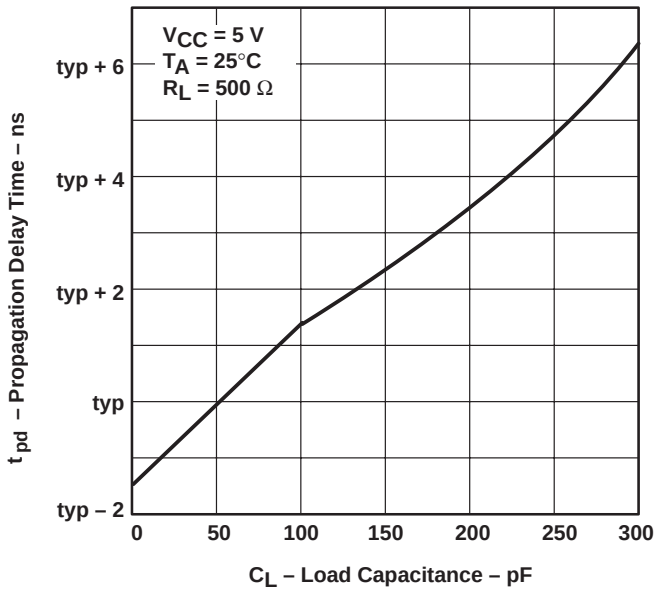


Figure 11

SUPPLY CURRENT vs CLOCK FREQUENCY

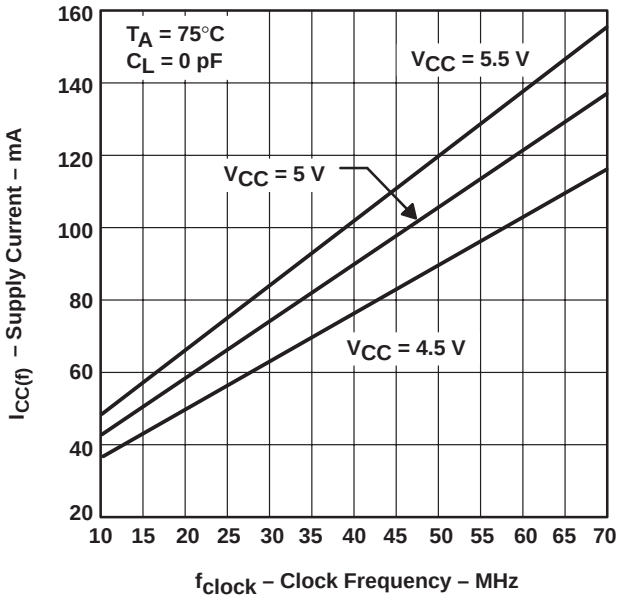


Figure 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-9470401QXA	LIFEBUY	CPGA	GB	84	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9470401QX A SNJ54ABT7819GB	
SNJ54ABT7819GB	LIFEBUY	CPGA	GB	84	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	5962-9470401QX A SNJ54ABT7819GB	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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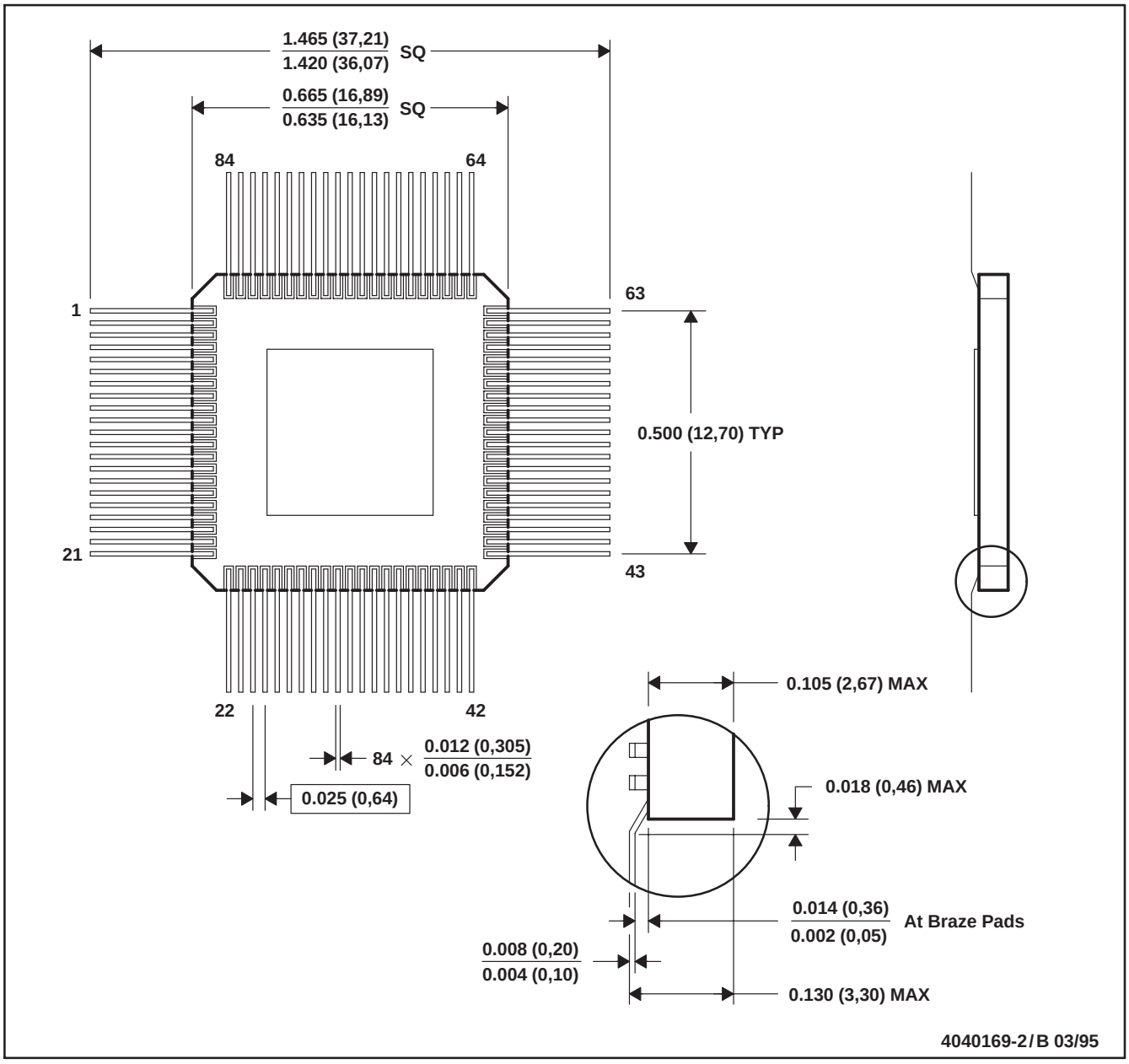
HT (S-CQFP-F84) **CERAMIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a metal lid.
D. The terminals are gold plated.
E. Falls within JEDEC MO-090 AA

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